

Remarks

Claims 1-5, 8, 10-16 and 18-20 were pending in the above-identified application when last examined. Claims 1-3 and 18 are amended to replace the conditional word “if” with “when.” Claims 1-5, 8, 10-16, and 18-20 are presented for reconsideration and allowance in view of the following remarks.

Claim Rejection under 35 U.S.C. § 101

The Examiner states that claims 1-5, 8, and 10-14 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Applicants respectfully traverse this rejection.

The Examiner on page 2 of the Final Office Action states that the steps of the method claims do not produce a useful, tangible, and concrete result. The Examiner further argues that the absence of a result does not indicate a result (pgs. 2 & 3, Final Office Action). Applicants respectfully disagree.

Since it is clearly indicated that when any error occurs a signal indicates an error, it is also clearly communicated that in the absence of a signal no error has occurred. In this context, the state when no error signal is communicated is a final result that is tangible.

In addition claims 1-3 have been amended to replace the conditional word “if” with “when.” Thus the Examiner’s argument (Final Office Action, pg. 2) that the Applicants’ claims language is broader than “if there is no error then do not signal” is moot.

Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 1-5, 8 and 10-14 under 35 U.S.C. §101.

Claim Rejection under 35 U.S.C. § 103(a)

The Examiner rejected claims 1-5, 8, 10-16, and 18-20 under 35 U.S.C. 103(a) as being unpatentable over Sharma (USP 6,412,046) and Dubey (USP 5,812,811).

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art cited must teach or suggest all the claim limitations. See M.P.E.P. § 2143. Without admitting that the first or second criteria are satisfied, Applicants respectfully assert that the Examiner's rejection fails to satisfy the third criteria.

Applicants continue to believe that the claims are allowable at least for the reasons set forth in the previous response, including that Sharma does not disclose or suggest determining whether generation of an event by an agent in response to a stimulus is conditional.

Claims 1, 15 and 20 disclose creating an expectation of an event, indicating that it is speculative, monitoring conditions relating to the event and either promoting the speculative expectation to a non-speculative expectation or deleting it, and finally determining whether the non-speculative event occurred and making sure the event for a deleted expectation did

not occur. Neither Sharma nor Dubey teach or suggest either together or individually creating an expectation of an event, indicating that it is speculative, monitoring conditions relating to the event and either promoting the speculative expectation to a non-speculative expectation or deleting it, and finally determining whether the non-speculative event occurred and making sure the event for a deleted expectation did not occur.

For example, the Examiner has referred to Sharma, Fig. 5 element 500 and the associated description as disclosing the deletion of a speculative expectation if conditions indicate that a speculatively expected event should not take place. Element 500 is a step in a process for verifying a cache prefetch mechanism. In step 500, a determination is made about whether a memory transaction is a fetch or a prefetch operation. See Sharma, col. 6, lines 51-54 and col. 7, lines 6-13:

“Fig. 5 is a flow chart illustrating finder processes for verifying the cache prefetch mechanism. The process begins at block 500, where the request is checked to be either a fetch or a prefetch.”

‘In block 500, if the transaction is a prefetch, the process moves to block 515, and the cache line address prefetched is checked to see if greater than or equal to the last cache line address prefetched. If not greater, the process moves to block 520, and an error flag is set. If greater than or equal, the process moves to block 535, where the last cache line address prefetched is set equal to the cache line address prefetched, the cache line address is marked as accessed, and the cache lines accessed is incremented.”

Neither Sharma nor Dubey either together or individually teach or suggest that speculative expectations are created and then either promoted or deleted. Please note that the speculative expectation of the claims is not merely a step in a verification process at which conditions indicate that some event may take place in the future, such as the

indication that a memory transaction has been received and determining whether that memory transaction is a fetch or a prefetch operation. For example, claim 1 recites detecting a stimulus, creating an expectation, indicating that the expectation is speculative, then promoting or deleting the expectation, and finally verifying whether any event related to the promoted or deleted expectation occurred properly.

The Examiner admits, on page 4 of the Office Action, that Sharma does not explicitly disclose: converting said speculative expectation to a non-speculative expectation if the conditions indicate that said event should be generated by said agent; deleting said speculative expectation if said conditions indicate that said event should not be generated by said agent. The Examiner further states that Dubey however discloses an analogous caching memory system having said features of converting and deleting. (pg. 4, Office Action).

Applicants respectfully disagree with the Examiner that Dubey discloses an analogous caching memory system having said features of converting and deleting. Nowhere in Dubey are the features “converting” or “deleting” mentioned let alone described with respect to a caching memory system. Furthermore, Dubey does not teach or suggest converting a speculative expectation to a non-speculative expectation if the conditions indicate that an event should be generated by an agent. Dubey does not teach or suggest deleting a speculative expectation if the conditions indicate that an event should not be generated by an agent.

In addition, Applicants believe that the caching memory system of Dubey is not

analogous to the expectation based event verification of this application. Dubey describes a central processing unit (CPU) in a computer that permits speculative parallel execution of more than one instruction thread (See Abstract). This invention teaches creating an expectation of an event, indicating that it is speculative, monitoring conditions relating to the event and either promoting the speculative expectation to a non-speculative expectation or deleting it, and finally determining whether the non-speculative event occurred and making sure the event for a deleted expectation did not occur. This method is used for verification of an agent, not actual operation of a CPU.

Applicants respectfully submit that claims 1, 15, and 20 patentably distinguish over the cited reference for at least the reasons above. Claims 2-5, 8, and 10-14 depend from claim 1 and are believed to patentably distinguish over the cited references for at least the above reasons. Claims 18-19 depend from claim 15 and are believed to patentably distinguish over the cited references for at least the above reasons. Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 1-5, 8, 10-16 and 18-20 under 35 U.S.C. §103(a).

Conclusion

Applicants respectfully submit that Applicants' pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby requested.

Respectfully submitted,

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